Specification Amendments

Please replace paragraph 004 with the following re-written paragraph:

004 Huang et al., U.S. patent No. 6,121,073 discloses a fuse structure and method of deleting redundant circuit elements on a semiconductor device. The fuse structure is useful in increasing the repair yield on RAM chips by deleting defective rows of memory cells. The method involves forming a fuse area in a patterned electrical circuit layer also used to form interconnections. The fuse may be a polysilicon layer. A relatively thin layer of about 0.1 micrometers of insulation is deposited having a uniform thickness across the substrate. The next level of patterned interconnections is formed with a portion of the layer aligned over the fuse area to serve as an etch-stop layer. The conducting layers can be first and second polysilicon layer on a RAM chip. The remaining multilevel of interconnections are then formed having a number of relatively thick entry-level dielectric layers interposed which can have varying thicknesses across the substrate. The fuse window[[s]] ~~were~~ openings are then selectively etched in the entry-level

dielectric layers to the etch stop layer and the etch stop layer is selectively etched in the fuse window to the insulating layer over the fuse area. The process allows fuse structures to be built without over etching and thereby causing fuse damage. The uniformly thick insulating layer allows repeatable and reliable laser evaporation to open the desired fuses.

Please replace paragraph 0017 with the following rewritten replacement paragraph:

0017 Fig. 2 illustrates a semiconductor device 50 with portions broken away according to the present invention. The semiconductor device 50 may include a base portion (not shown) with discrete devices formed therein. The semiconductor device 50 may also includes an oxide or low dielectric material 52 including a number of discrete semiconductor structures (not shown) formed therein. A multilayer structure may be formed over the oxide or low dielectric material 52 including a plurality of dielectric layers 56 which may be silicon dioxide, or may be a low dielectric material such as polyimide nanoforms or porous glasses. An etch-stop layer 54 such as silicon nitride may be positioned between adjacent layers of dielectric material. A damascene structure 58 is provided in the dielectric material and

includes at least a first (first from the topmost metallization layer) metallization layer 60, a plug 62 and a topmost (second) metallization layer 64 which may be the top metallization layer. The top metallization layer 62 may have a thickness of about 9000 angstroms or more. A fuse 66 is formed on the topmost metallization layer 64. Preferably the fuse is aluminum material formed at a thickness of about 1000-7000 angstroms and preferably 3500 angstroms. The fuse may be formed by an additional masking step using a patterned photoresist layer with an opening therein through which the aluminum may be deposited on top of the top metallization layer 64 by electroplating, screening or other methods known to those skilled in the art. An additional passivation layer 68 may be provided over the multilayer structures and may be a single layer or a layer of plasma enhanced silicon nitride to a thickness of about 750 angstroms and a layer of plasma enhanced oxide to a thickness of about 4000 angstroms. Additional passivation layers 72, 74 may also be provided and may be a layer of plasma enhanced oxide to a thickness of about 4000 angstroms and layer of plasma enhanced silicon nitride to a thickness of about 6000 angstroms. A fuse window 76 is provided through the passivation layers down to the fuse passivation layer 68. The fuse 66 may be blown by energizing the fuse with a laser through the fuse passivation

layer 68. Preferably when the dielectric layers 52, 56 are a low dielectric material, a laser beam is utilized to blow the fuse. The low dielectric material layers 52, 56 may have a dielectric constant k ranging from 2.0-3.6 and preferably from 2.2-3.0. The combination of a low dielectric and a thick top metal layer such as a copper damascene structure with a low-k dielectric increases the chance of having lower corner cracks and copper fuse residue due to the low-k dielectric softness. Lower corner cracking may produce unclean link removal and damage to the circuit. Consequently, metal links are cut more effectively at lower nominal energies and less likely to have lower corner cracking beneath the fuse link.